

MEMORY CELL WITH TIGHT COUPLING

This application is a Continuation of U.S. Application No. 09/516,681, filed March 1, 2000, which is incorporated herein by reference.

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Field of the Invention

This invention relates to information storage, and more particularly to solid state memory used in information storage systems.

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Background of the Invention

A modern information storage system should acquire information quickly, maintain the information with integrity over time, and provide for the quick and accurate retrieval and erasing of the information. As the demand for miniature hand held communication and other data processing devices increases, the demand for smaller nonvolatile data storage devices increases. A flash memory device, such as erasable programmable read only memory (EPROM) or an electrically erasable programmable read only memory (EEPROM), is one type of information storage device used in modern nonvolatile information storage systems.

Figure 1 is a cross-sectional view of a prior art flash memory cell 100. Flash memory cell 100 includes substrate 103, source region 106, drain region 109, channel 112, oxide 115, floating gate 118, dielectric layer 121, and control gate 124. Dielectric layer 121 comprises a three layer oxide-nitride-oxide dielectric.

In flash memory cell 100, information is stored on floating gate 118 as electronic charge. To facilitate the quick acquisition of information in flash memory cell 100, the cell is designed to have a large capacitance between control gate 124 and the floating gate 118. As the density of memory cells in a solid state memory is increased by scaling the physical dimensions of the cells, the area of floating gate 118 is decreased, which decreases the capacitance and coupling between control gate 124 and floating gate 118. Unfortunately, this decrease in coupling reduces the electric field between the substrate and the floating gate during a write operation. A decrease in the

electric field decreases the rate at which hot electrons flowing in channel 112 are injected onto floating gate 118 and increases the time to store charge on the floating gate 118.

Information must be retained in flash memory cell 100 on floating gate 118 for a long period of time. As described above, as flash memory cells are scaled, the area of the floating gate in each cell is decreased and the capacitance between the floating gate and the control gate is decreased. A smaller capacitance results in less charge being injected into the floating gate. For a particular leakage current, a memory cell having less stored charge loses its information more quickly than a memory cell having more stored charge. One solution to this problem is to substitute a material having a high dielectric constant for dielectric 121 in flash memory cell 100. Unfortunately, materials that have a high dielectric constant and are compatible with integrated circuit manufacturing processes often have a high leakage current, which decreases the storage lifetime of the stored information for a fixed amount of charge.

Quick and accurate retrieval of information from flash memory cell 100 requires accurately sensing the charge stored on floating gate 118. A large amount of stored charge provides a signal that is easier to accurately sense than a small amount of stored charge. A large amount of stored charge also decreases the read time at the sensing device. Unfortunately, as devices are scaled to a small fraction of a micron, and the operating voltages are reduced, the charge on floating gate 118 is often decreased, thus making the quick and accurate retrieval of information more difficult. Flash memories already operate with relatively little stored charge, so as the stored charge is decreased further by scaling the physical dimensions of a memory cell, there is an increase in the number of errors at the sense amplifier when reading information from the scaled flash memory cell 100.

For these and other reasons there is a need for the present invention.

Summary of the Invention

The above mentioned problems with flash memory cells and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

5 A memory cell or nonvolatile memory cell having a dielectric sandwich, insulating sandwich, or coupling dielectric that is capable of increasing the coupling in the memory cell is disclosed. The dielectric sandwich is thin and has at least one high permittivity layer having a thickness of between about 140 and 240 angstroms. The dielectric sandwich also has at least one oxide layer formed at a temperature above the
10 crystallization temperature of the high permittivity layer. In the flash memory cell, the dielectric sandwich is located between the control gate and the floating gate and provides for tight coupling between the control gate and the floating gate.

Brief Description of the Drawings

15 Figure 1 is a cross-sectional view of a prior art flash memory device.

Figure 2 is a cross-sectional view of some embodiments of a flash memory device of the present invention.

Figure 3 is a block diagram of a system level embodiment of the present invention.

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Detailed Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be
25 practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present
30 invention is defined only by the appended claims.

Figure 2 is a cross-sectional view of some embodiments of memory cell 200 of the present invention. Memory cell 200 comprises substrate 203, insulator 206, floating gate 209, dielectric sandwich 212, and control gate 215.

Substrate 203, in one embodiment, is a semiconductor, such as germanium or silicon. Alternatively, substrate 203 is gallium arsenide, silicon-on-sapphire, or any other crystalline or amorphous material suitable for use as a substrate in the manufacture of integrated circuits. Substrate 203, in one embodiment, is fabricated from an n-type silicon having a pair of spaced apart p+ source 218 and p+ drain 221 regions. Channel 224 is located between source 218 and drain 221 regions.

Insulator 206 is formed above substrate 203 and has thickness of less than 1000 angstroms. Increasing the thickness of insulator 203 above 1000 angstroms decreases the capacitance between the floating gate and the substrate and between the control gate and the substrate, which increases the time to store charge on the floating gate. In one embodiment, insulator 206 is a thermal oxide, such as silicon oxide, formed by oxidizing substrate 203. The present invention is not limited to a particular form of silicon oxide. Both SiO and SiO₂ are suitable for use in connection with the present invention.

Floating gate 209 is formed above insulator 206. In one embodiment, floating gate 209 is polysilicon, and is deposited using a chemical vapor deposition (CVD) process or other suitable process to a thickness of about 2000 angstroms. Floating gate 209, in one embodiment, is doped to a desired level by diffusing phosphorous into the polysilicon.

Dielectric sandwich 212 is formed above floating gate 209. Dielectric sandwich 212 comprises a plurality of layers. In one embodiment, dielectric sandwich 212 comprises four layers including oxide layer 227, tantalum oxide layer 230, cell nitride layer 236, and wetgate oxide layer 239.

Oxide layer 227 is formed above floating gate 209. In one embodiment, oxide layer 227 is SiO₂ thermally grown to a thickness of between about 28 angstroms and 32 angstroms on floating gate 209. A thickness of less than about 23 angstroms increases the charge leakage in the dielectric sandwich and a thickness of greater than about 32 angstroms unnecessarily decreases the capacitance of dielectric sandwich 212.

Alternatively, oxide layer 227 may be formed on floating gate 209 by chemical vapor deposition (CVD). Forming oxide layer 227 by CVD permits floating gate 209 to have a higher doping level than growing oxide layer 227 thermally.

5 Tantalum oxide layer 230 is formed above oxide layer 227. In one embodiment, tantalum oxide layer 230 is tantalum pentoxide, Ta_2O_5 , deposited by metal organic chemical vapor deposition (MOCVD) to a thickness of between 60 and 100 angstroms. A thickness of greater than 100 angstroms decreases the capacitance of the dielectric sandwich, which degrades the performance of the memory cell during a charging operation. A thickness of less than about 60 angstroms increases the charge leakage in
10 dielectric sandwich 212. Other high dielectric materials or high permittivity materials having a permittivity of between ten and twelve are also suitable for use in connection with the present invention. For example, Al_2O_3 is suitable for use in connection with the present invention. An advantage of employing a high dielectric material, such as tantalum oxide, in dielectric sandwich 212 is that the coupling between the control gate
15 and the floating gate is increased, and increased coupling allows faster charging of floating gate 209 by creating a stronger field and faster charging of floating gate 209 during a write operation.

Tantalum oxide layer 230, in one embodiment, is reoxidized by rapid thermal processing (RTP) at a temperature of between about 400 degrees centigrade and about
20 900 degrees centigrade. In one embodiment, tantalum is oxidized above the crystallization temperature. In an alternate embodiment, where subsequent processing occurs at temperatures above 750 degrees centigrade, an amorphous tantalum oxide can be used, and reoxidation, in this embodiment, is kept below about 725 degrees centigrade. An advantage of reoxidizing the tantalum oxide layer is that reoxidizing
25 typically reduces leakage.

Cell nitride layer 236 is formed above tantalum oxide layer 230. In one embodiment, cell nitride layer 236 is Si_3N_4 and has a thickness of between about 40 and 60 angstroms. A thickness of less than about 40 angstroms increases charge leakage in dielectric sandwich 212 and a thickness of more than about 60 angstroms unnecessarily
30 decreases the capacitance of dielectric sandwich 212. Capacitor uniformity across the

memory cell is dependent on the uniformity of nitride layer 236. Low pressure chemical vapor deposition is one method of depositing cell nitride layer 236.

Wetgate oxide layer 239 is formed above cell nitride layer 236. In one embodiment, wetgate oxide layer 239 is SiO₂ and has a thickness of between about 10 and 50 angstroms.

Control gate 215 is formed above dielectric sandwich 212. Control gate 215 is formed from polysilicon. Control gate 215 may include other conductive materials, such as aluminum, and is deposited to a depth of about 2000 angstroms. Control gate 215 is doped to the desired level through phosphorous diffusion.

Dielectric sandwich 212, as shown in Figure 2, is formed between floating gate 209 and control gate 215 for use in connection with flash memory cell 200. However, dielectric sandwich 212 is not limited to use in a particular integrated circuit structural configuration. Dielectric sandwich 212 is useful in connection with any integrated circuit device that benefits from a dielectric composite that has a high capacitance value, a low leakage value, and is formed using conventional integrated circuit processing methods. Dielectric sandwich 212 may also be referred to as a floating gate coupling dielectric.

Memory cell 200, in one embodiment of the present invention, has a gate dimension area of about 1 micron. To charge flash memory cell 200 having a gate dimension of about 1 micron, about 12 volts is applied to the control gate, and a pulse voltage of about 5 volts is applied between source 218 and the drain 221 regions. The width of the pulse voltage is selected to provide an amount of charge to floating gate 209 that generates a strong signal to the memory cell sense amplifier.

To summarize, in accordance with the present invention, the plurality of dielectric layers or dielectric sandwich 212 formed above floating gate 209 has a thickness greater than about 140 angstroms. The reason for fabricating a thin dielectric sandwich is to provide a large capacitance value between control gate 215 and the floating gate 209. A large capacitance value is desirable because it permits flash memory cell 200 to be scaled and to operate with a smaller control gate voltage and a smaller floating gate area, which facilitates the quick acquisition of charge, and the long term storage and accurate sensing of charge on floating gate 209. Dielectric sandwich 212, in one embodiment, has a

permittivity of between ten and twelve. Again, having a dielectric with a permittivity of between ten and twelve between control gate 215 and floating gate 209 permits the use of a lower gate voltage and a smaller cell size having a smaller floating gate area. In an alternate embodiment, the insulating sandwich has a thickness of between 140 angstroms and 240 angstroms and has a capacitance of 25% to 35% greater than an oxide-nitride-oxide insulator having a thickness of between 140 angstroms and 240 angstroms.

Referring to Figure 3, a block diagram of a system level embodiment of the present invention is shown. System 300 comprises processor 305 and memory device 310, which includes memory cells of one or more of the types described above in conjunction with Figures 2. Memory device 310 comprises memory array 315, address circuitry 320, and read circuitry 330, and is coupled to processor 305 by address bus 335, data bus 340, and control bus 345. Processor 305, through address bus 335, data bus 340, and control bus 345 communicates with memory device 310. In a read operation initiated by processor 305, address information, data information, and control information are provided to memory device 310 through busses 335, 340, and 345. This information is decoded by addressing circuitry 320, including a row decoder and a column decoder, and read circuitry 330. Successful completion of the read operation results in information from memory array 315 being communicated to processor 305 over data bus 340.

Conclusion

An embodiment of a nonvolatile memory cell has been described which has a high dielectric constant sandwich located between the control gate and the floating gate. The high dielectric constant sandwich also exhibits low charge leakage. A method of fabricating the nonvolatile memory cell has also been described.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.